HT6542B

Keyboard Controller with PS/2

Features

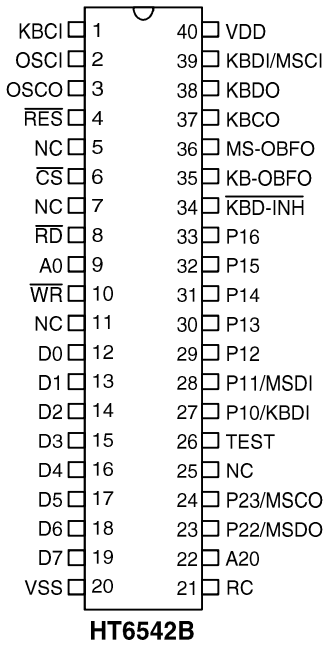
- High reliability MOS technology
- 8042-type host interface
- 6MHz-12MHz operating frequency
- Communicates with keyboard directly
- Provides enhanced Gate A20 switching
- Support PS/2 compatible mouse
- Auto-detect AT and PS/2 motherboard
- Support 40 pin DIP and 44 pin PLCC packages

General Description

The HT6542B is a keyboard controller developed by Holtek with a 4-bit microprocessor. It is pin-to-pin compatible with Intel 8042 keyboard controller used in IBM PC's. PC manufacturers need not modify any printed wiring layout when using the HT6542B in lieu of the Intel 8042 based keyboard controller. Furthermore, the HT6542B can support a system clock speed of up to 12MHz. The HT6542B can detect the motherboard type automatically, therefore it can be employed on both of AT and PS/2 motherboard.

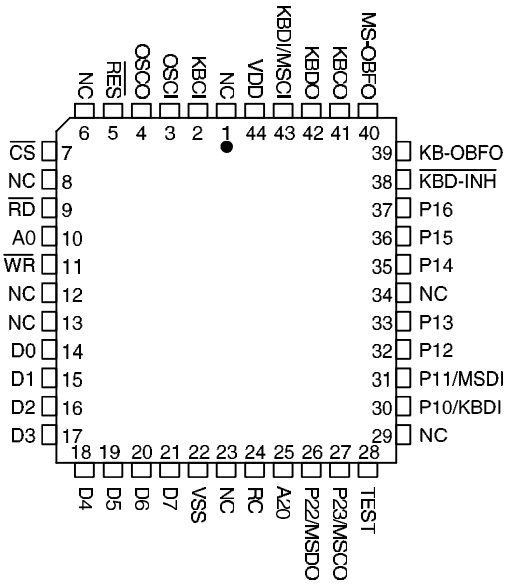
Pin Assignment

40 Pin DIP package



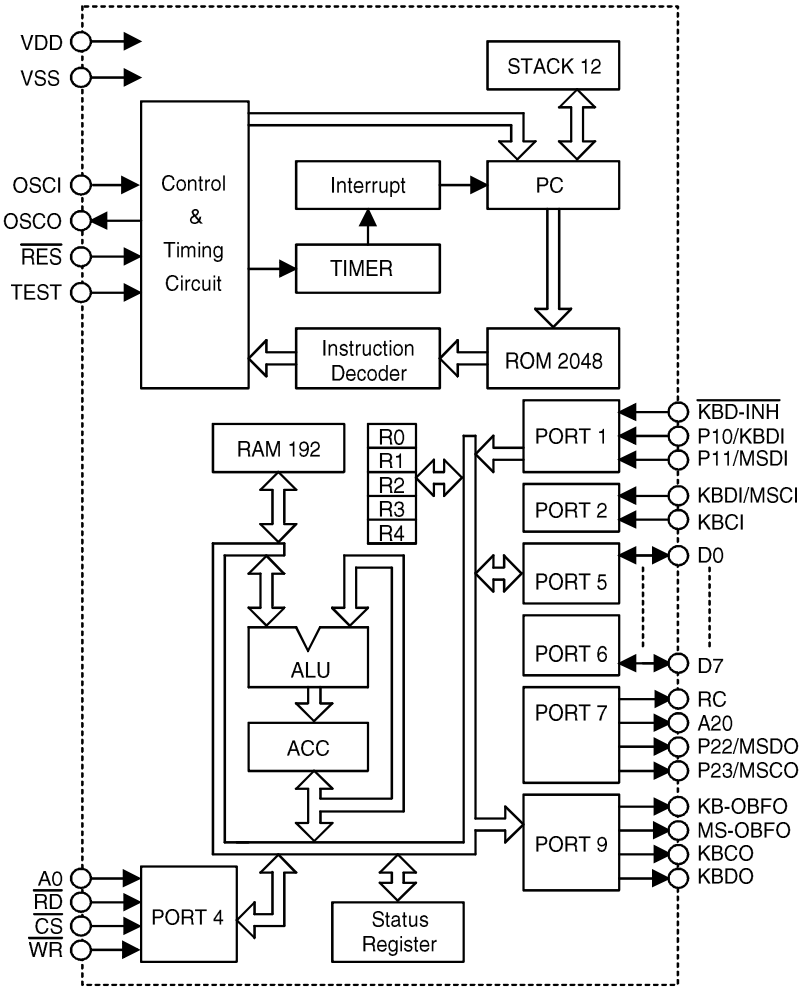
HT6542B

44 Pin PLCC package



This datasheet has been downloaded from http://www.digchip.com at this page

Block Diagram



Pin Description

Pin No. (DIP)	Pin No. (PLCC)	Pin Name	I/O	Pin Descriptions
1	2	KBCI	I	Keyboard clock input pin
2,3	3,4	OSCI,OSCO	I	System clock input pin, to generate internal oscillator signal
4	5	$\overline{RES}$	I	Low level to reset HT6542B. After $\overline{RES}$ goes to high level HT6542B needs 10ms to initial internal circuit
5,7,11,25	1,6,8,12,13, 23,29,34	NC	—	No connection
6	7	$\overline{CS}$	I	Host-interface chip select, active low
8	9	$\overline{RD}$	I	Host-interface read signal, active low
9	10	A0	I	Host-interface address select input. When high, it selects the command/status registers; when low it selects the data register

Pin No. (DIP)	Pin No. (PLCC)	Pin Name	I/O	Pin Descriptions
10	11	$\overline{WR}$	I	Host-interface write signal, active low
12~19	14~21	D0~D7	I/O	Host interface data bus. An 8-bit bi-directional port for data transfers between the host CPU and the HT6542B
20	22	VSS	—	Circuit ground
21	24	RC	O	Host-reset control signal output
22	25	A20	O	Gate A20 control signal output
23	26	P22/MSDO	I/O	General purpose input/output pin for AT motherboard. Mouse data output pin for PS/2 motherboard
24	27	P23/MSCO	I/O	General purpose input/output pin for AT motherboard. Mouse clock output pin for PS/2 motherboard
26	28	TEST	I	Test input pin, for IC test only. Connected to VCC in applications
27	30	P10/KBDI	I/O	General purpose input/output pin for AT motherboard. Keyboard data input pin for PS/2 motherboard
28	31	P11/MSDI	I/O	General purpose input/output pin for AT motherboard. Mouse data input pin for PS/2 motherboard
29~33	32~33 35~37	P12~P16	I/O	General purpose input/output pins
34	38	$\overline{KBD\text{-}INH}$	I	Keyboard inhibit input. When low, keyboard is inhibited. When high, keyboard transmission is enabled.
35	39	KB-OBFO	O	Keyboard output buffer full interrupt for AT and PS/2 mother board (active high)
36	40	MS-OBFO	O	Output low for AT mothboard. Mouse output buffer full interrupt for PS/2 mother board (active high).
37	41	KBCO	O	Keyboard clock output pin for AT and PS/2 motherboard.
38	42	KBDO	O	Keyboard data output pin for AT and PS/2 motherboard.
39	43	KBDI/MSCI	I	Keyboard data input pin for AT motherboard Mouse clock input pin for PS/2 motherboard
40	44	VDD	—	Positive power supply

Absolute Maximum Ratings

Supply Voltage ..... –0.3V to 5.5V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... 0°C to 70°C

D.C. Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	–	4.75	5	5.25	V
I_{DD}	Operating Current	5V	F_{OSC}=8MHz No load	—	4	6	mA
V_{IL}	Input Low Voltage	—	—	–0.5	—	0.8	V
V_{IH}	Input High Voltage	—	—	2	—	V_{DD}	V
V_{OL}	P10~P16, KBCI, KBDI, D0~D7, RC, A20, P22, P23, KB-OBFO, MS-OBFO Output Low Voltage I_{OL}=6mA	5V	V_{OL}=0.5V	—	—	0.5	V
V_{OH}	D0~D7, KB-OBFO, MS-OBFO, KBCO, KBDO, A20, RC Output High Voltage I_{OH}=0.3mA	5V	V_{OH}=4.5V	4.5	—	—	V
R_{PH1}	P10~P16, $\overline{\text{KBD-INH}}$ Pull-High Resistance	—	—	10	20	30	KΩ
R_{PH2}	KBCI, KBDI, $\overline{CS}$, $\overline{RD}$, A0, $\overline{WR}$ Pull-High Resistance	—	—	30	50	70	KΩ

Functional Description

Power on

When power is switched on, the HT6542B auto-detect the motherboard type(AT or PS/2), then disable the keyboard/mouse and waits for the self-test command to perform a self-test. If no error is detected during self-test, HEX 55 is registered in the output buffer (note that any value other than HEX 55 would indicate HT6542B failure) and the keyboard interface is enabled. The HT6542B is now ready to receive a system command or keyboard data.

Keyboard/mouse data transmission

The keyboard/mouse transmits data to the controller in an 11-bit format in sync, with the keyboard/mouse clock signal. If this transmission is not completed within the specified period, the HT6542B will register HEX FF into the output buffer and set the "transmit time-out" error bit in the STATUS REGISTER to 1.

Controller data transmission

The controller transmits data to the keyboard/mouse in the same manner as it receives data from the keyboard/mouse. When the HT6542B starts transmitting data and the keyboard/mouse does not start receiving (does not start clocking) or data transmission is not completed within 15ms, the HT6542B will register HEX FE into the output buffer and set the "transmit time-out" error bit in the STATUS REGISTER to 1.

Keyboard inhibited ($\overline{\text{KBD-INH}}$ to low)

If the $\overline{\text{KBD-INH}}$ is switched to low, the keyboard/mouse is inhibited. The HT6542B receive keyboard/mouse code and check the $\overline{\text{KBD-INH}}$ status, if inhibited the keyboard SCAN CODE and mouse code will be ignored and the keyboard/mouse command response is registered into the HT6542B's output buffer.

Status register notations

The STATUS REGISTER is located in HEX 64 of the I/O. It provides the HT6542B and interface status to the system. The following are the definitions for each bit:

- b0(OBF): Output buffer full

  This bit is set while the HT6542B is sending data to the output buffer and cleared when the system reads the output buffer(I/O HEX 60H).

- b1(IBF): Input buffer full

  This bit is set while the system is sending data to the HT6542B's input buffer and cleared when the HT6542B reads the input buffer data.

- b2: System flag

  This bit is 0 after power-on reset, set to 1 after self-test OK.

- b3: Command/Data

  When the system writes the data to the HT6542B from I/O 64H, this bit becomes 1. Reset to 0 if from I/O 60H.

- b4:

  This bit reflects the $\overline{\text{KBD-INH}}$ status whenever data is placed in the HT6542B's output buffer.

- b5: Auxiliary Output Buffer Full.

  0: The HT6542B's output buffer is a keyboard data.
  1: The HT6542B's output buffer is a mouse data.

- b6: Transmit time-out

  Set to 1 when the keyboard or mouse is not able to completely transmite data to the HT6542B within the specified period.

- b7: Parity error

  1: The HT6542B has received the keyboard/mouse code with a parity error. (should be odd parity).

Output buffer

The output buffer is located in I/O HEX 60. It is used to transmit keyboard/mouse code or keyboard controller response data. The output buffer data is valid only when OBF=1.

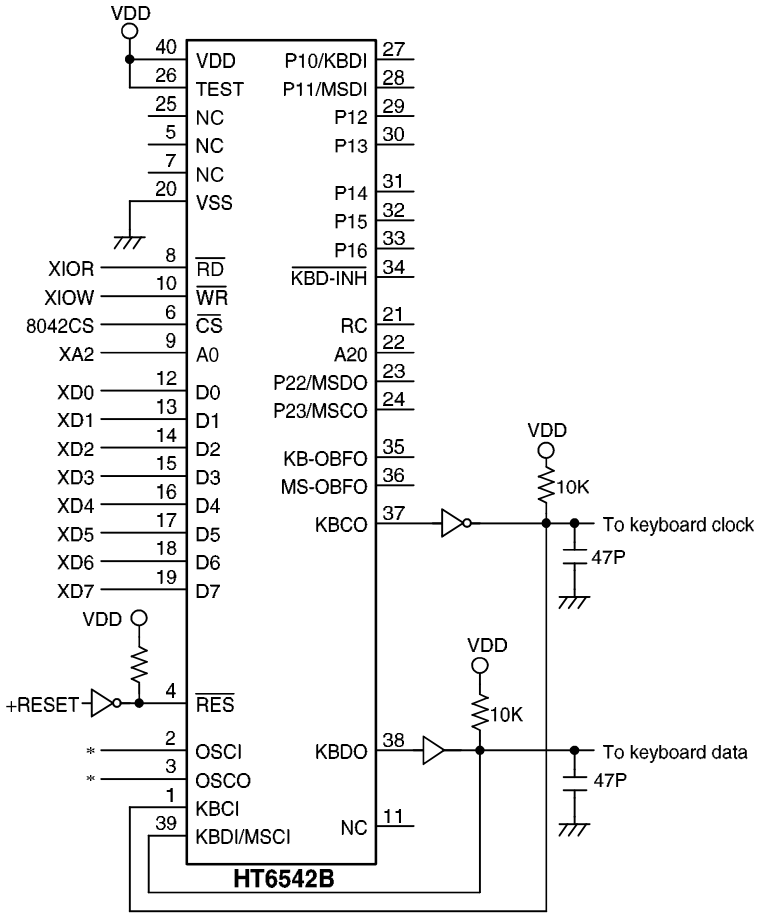
Input buffer

The input buffer is located in I/O HEX 60 or HEX 64. The system writes command and data into this port in the following categories:

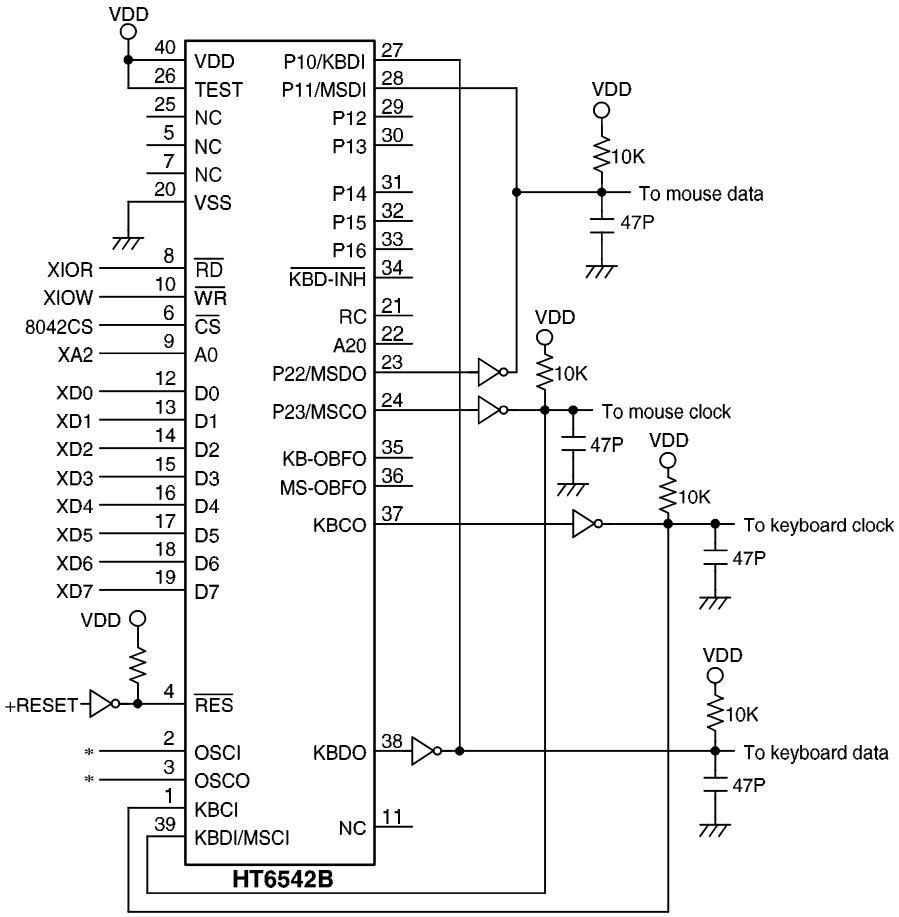
- Data written to I/O HEX 64 as command write.
- Data written to I/O HEX 60 as data write.

Application Circuit

For AT motherboard (40 pin DIP, for example)



For PS/2 motherboard (40 pin DIP, for example)



* OSCI, OSCO connection

